AMENDMENTS TO THE SPECIFICATION

At page 1, paragraph 2, starting on line 11, please change to read as follows:

To improve network reliability against failures, the following methods ~~means~~ have

conventionally been applied in an ATM network, where a protection channel is provided in

addition to a working channel.

At page 6, paragraph 1, starting on line 2, please change to read as follows:

Each node consists of an ATM switching system which is provided with the following

elements: an ATM switch circuit (SW) 1 for performing a cell switching function; external line

interface portions (LINF) 2' – 1 to 2' –n for inserting cells, ~~located at~~ to be output to an ~~the~~

external line side; and internal line interface portions (LINF) 2-1 to 2-n for extracting cells,

~~located at the internal line side~~ transmitted from the external line.

At page 6, paragraph 2, starting on line 8, please change to read as follows:

Also, there are provided in each node a multiplexer (MUX) 3-1 for multiplexing input

ATM cells extracted by the internal ~~input from~~ line interface portions 2-1 to 2n, interfacing with

ATM switch circuit 1; a demultplexer (DMX) 3-2 for demultiplexing multiplexed ATM cells,

also interfacing with ATM switch circuit 1; and a controller 4 for performing overall control

function.

At page 7, paragraph 1, starting on line 1, please change to read as follows:

(3) Controller 4 orders (control command) ~~to switch over the connection (ACT) for the~~

~~APS. Specifically, controller 4 orders ATM switch circuit 1 to switch over from~~ the ATM

switch circuit 1 to switchover from an internal line interface portion, ~~(LINF) 2-1~~ where the

working channel is terminated, to another internal line interface portion ~~(LINF) 2-i~~ where the

protection channel is terminated, by designating the connection for the APS (from (1) above).
More specifically, using a function provided in each internal line interface portion (LINF) 2-1 to
2-n, an ACT bit in each ATM cell header in transmission is set either 'ON' (which or 'OFF'.
The ACT bit denotes the internal line interface portion 2-i i.e. the protection channel side is in
working state), or 'OFF' (which denotes line interface portion 2-1 i.e. the working channel side
is in working state) where the protection channel is terminated when set 'ON', or denotes the
internal line interface portion where the working channel is terminated when set 'OFF'.

At page 8, paragraph 4, starting on line 9, please change to read as follows:

In FIG. 3, a functional element functional elements of demultiplexer (DMX) 3-2 provided
in each node is are shown.

At page 8, paragraph 5, starting on line 11, please change to read as follows:

In this FIG. 3, Tag-B is a tag provided in an ATM cell header for identifying an output
channel. O-ICID-A is also provided in the ATM cell header, which is an 'internal 'a channel
identifier' for identifying a channel in the output channel indicated by Tag-B.

At page 8, paragraph 7, starting on line 19, please change to read as follows:

The tag and the internal channel identifier explained above are set into an ATM cell
header at either line interface portions 2-1 to 2-n and 2'-1 to 2'-n, multiplexer (MUX) 3-1, or
ATM switch circuit 1, under the control of controller 4.

At page 8, last paragraph, starting on line 23, please change to read as follows:

For example, in node C shown in FIG. 3, an APS identifier in provided in the ATM cell

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header of an ATM cell input to demultiplexer (DMX) 3-2 is examined in a circuit 300. If this APS identifier indicates the cell is the object for ~~the~~ APS processing (i.e. APS is 'ON'), then a cell duplication table 30 is referred to, using Tag-B and O-ICID-A, which are also derived from the ATM cell header in the circuit 300 as the reference keys or address codes for accessing.

At page 9, paragraph 2, starting on line 10, please change to read as follows:

In FIG. 4, there is illustrated a configuration block diagram of, for example, line interface portion ~~2-i~~ 2-1 on the internet line side at which ~~is provided~~ the ATM cell is input, in node D, for example, located in the downstream direction against node C. In this FIG. 4, O-VPI/VCI is stored in a cell header, showing a value of VPI/VCI (virtual path and virtual channel identifier) of an output line related to the cell, and is detected in the cell header by a circuit 210.

At page 9, paragraph 3, starting on line 18, please change to read as follows:

Using as a reference key or address code, an internal line and a channel identifier O-ICID-A, which is detected from the cell header of ~~in~~ an input ATM cell in a circuit 210, a VPI/VCI conversion table 21 is referred to. Then, VPI/VCI to be forwarded to an ~~external~~ output line is obtained from VPI/VCI conversion table 21.

At page 9, last paragraph, starting on line 26, please change to read as follows:

Also, in line interface portion ~~2-i~~ 2-1 on the internal line side, there is provided an alarm cell insertion circuit 20 to insert an alarm cell named VP/VC-AIS. When a failure occurs between node C and node D, and node D detects this failure, an alarm cell is inserted according to a control command issued from controller 4.

At page 10, paragraph 2, starting on line 10, please change to read as follows:

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In FIG. 5, there is shown a block diagram of a configuration example related to the input side of line interface portion 2-1 in node F which constitutes a terminal node of a protected domain. ~~By referring to an ICID conversion table 23 using VPI/VCI, which is an external virtual~~ ~~path and virtual channel identifier stored in a header of an input ATM cell, as a reference key,~~ An ICID conversion table 23 is referred to by using as a reference key, VPI/VCI, which is an external virtual path and virtual channel identifier detected in a circuit 230 from a header of an input ATM cell, and then a corresponding internal virtual path and virtual channel identifier, I-ICID-A, is obtained.

At page 10, paragraph 3, starting on line 18, please change to read as follows:

The reason ~~of~~ for the above processing is that VPI/VCI is composed of 22 bits and requires a large ~~amount~~ number of circuits to process in ATM switch circuit 1. Therefore, VPI/VCI is converted into I-ICID-A which is a condensed form of the internal path and channel identifier. A header modification portion 24 replaces VPI/VCI with the obtained I-ICID-A in an ATM cell header ~~which~~.

At page 11, paragraph 2, starting on line 6, please change to read as follows:

Values in ~~those~~ tables 25 and 26 for determining that a cell is an object for the APS etc. are set by ~~an order~~ a control command from controller 4 either in advance or ~~in case~~ as necessary.

At page 11, paragraph 5, starting on line 15, please change to read as follows:

In ~~FIG. 6,~~ FIG. 5, setting for ~~there is shown an embobidment for setting~~ the APS identifier set table 25 and the ACT bit set table 26 ~~by an order from controller 4 which~~ is carried out by an order (command) from controller 4 in a procedure after the APS is started. ~~The~~

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~~embodiment intends to shorten the required time for an APS switchover by setting ACT bit set table 25 with high-speed.~~ Fig. 6 shows a configuration of an embodiment to set the APS identifier set table 25 and the ACT bit set table 26 with high-speed so that the required time for an APS switchover can be shortened.

At page 11, paragraph 6, starting on line 21, please change to read as follows:

A 17

In FIG. 5, when an APS switchover occurs, it is necessary to rewrite all data related to the corresponding connection in the APS identifier set table 25 and the ACT bit set table [[25]] 26, which may necessitate large processing time.

At page 11, last paragraph, starting on line 25, please change to read as follows:

A 18

On the other hand, according to the configuration shown in FIG. 6, a ~~table 25 is~~ tables 25 and 26 are provided for use of setting APS bits and ACT bits at the unit of an APS group (APS-Gr.). This enables the setting of ~~to set~~ the tables ~~table~~ from controller 4 at the unit of APS group i.e. in a batch of lines, instead of individual line by line, with less processing time.

At page 12, paragraph 1, starting on line 4, please change to read as follows:

A 19

In order to refer to ~~this table 25~~ these tables 25 and 26, information is required to identify which APS group each connection belongs to. For this purpose, an APS group conversion table 29 is provided for obtaining APS-Gr from I-ICID-A having been extracted from ICID conversion table 23. Each APS group is generally assigned corresponding to each outgoing line of ATM switch circuit 1.

At page 12, paragraph 2, starting on line 10, please change to read as follows:

A 20

Using an APS group obtained from APS group conversion table 29, an APS identifier set

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CONT

A 26

table ~~26~~ <u>25</u> is referred to. Also ACT bit set table ~~25~~ <u>26</u> is referred to using an APS group

obtained from APS group conversion table 29.